



Sierra Components, Inc.

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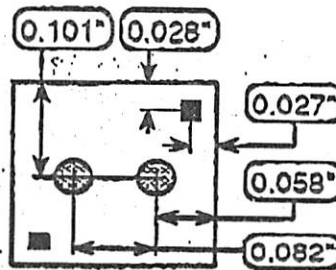
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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below.

Die Size = .199" x .203"

 Source Pads = .035" Dia.

 Gate Pads = .019" x .019"



Topside Metal: Aluminum

Backside: TiNiAG

Backside Potential:

Mask Ref:

Bond Pads (Mils): As Above

APPROVED BY:

MFG: Advanced Power Tech

DIE SIZE: .199" X .203"

THICKNESS: .018"

DATE: 11/2/99

P/N: APT601R3DN

DG 10.1.2

Rev A 3-4-99